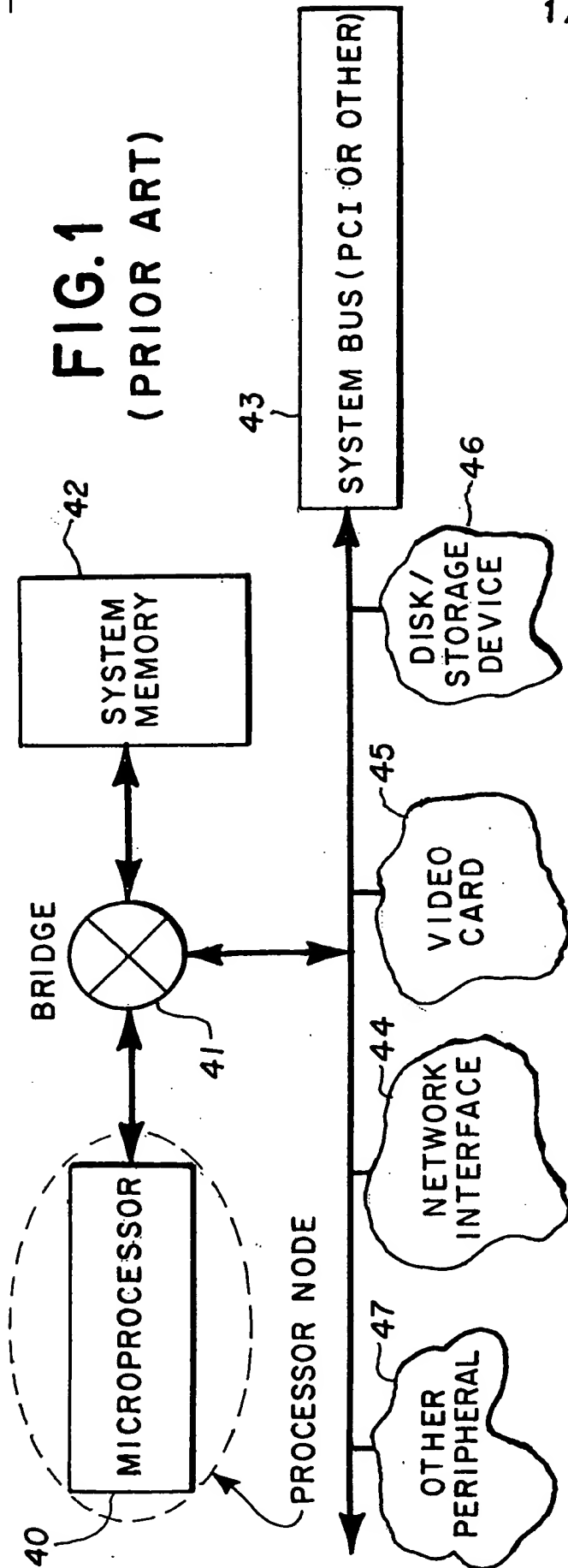
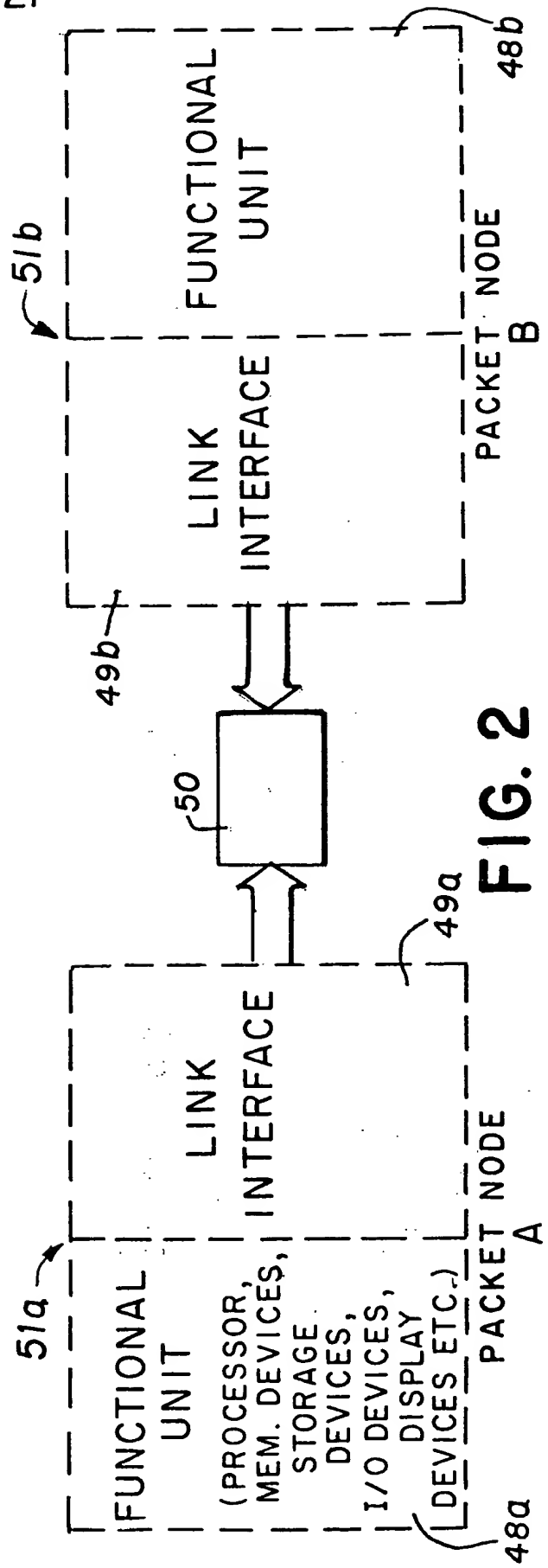


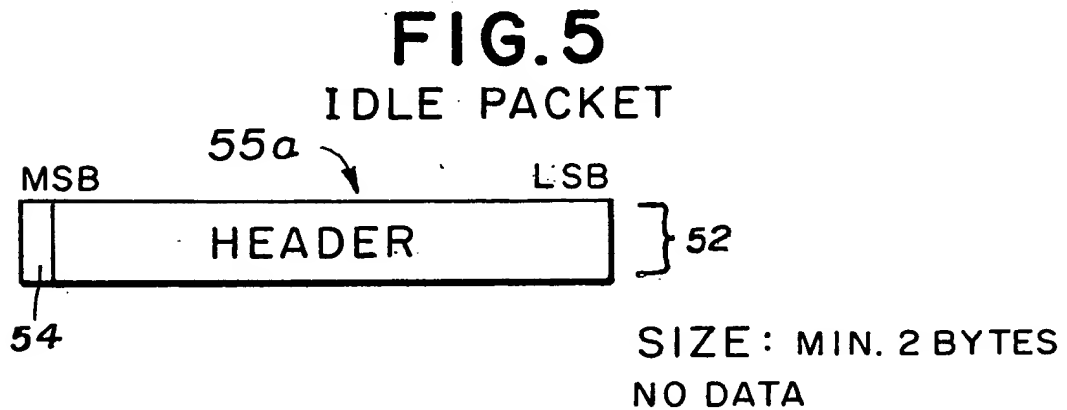
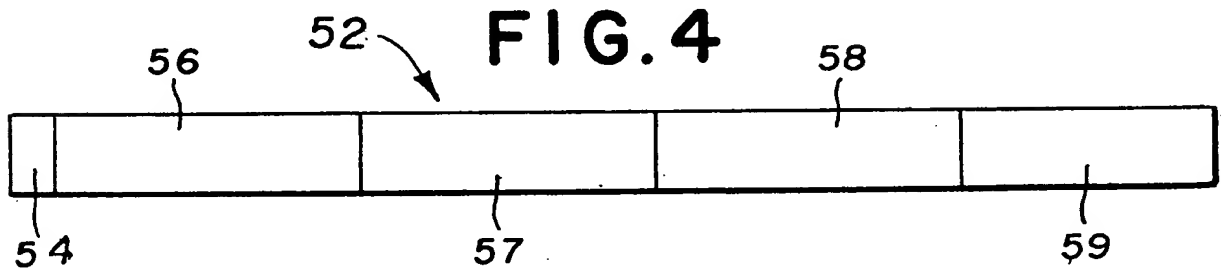
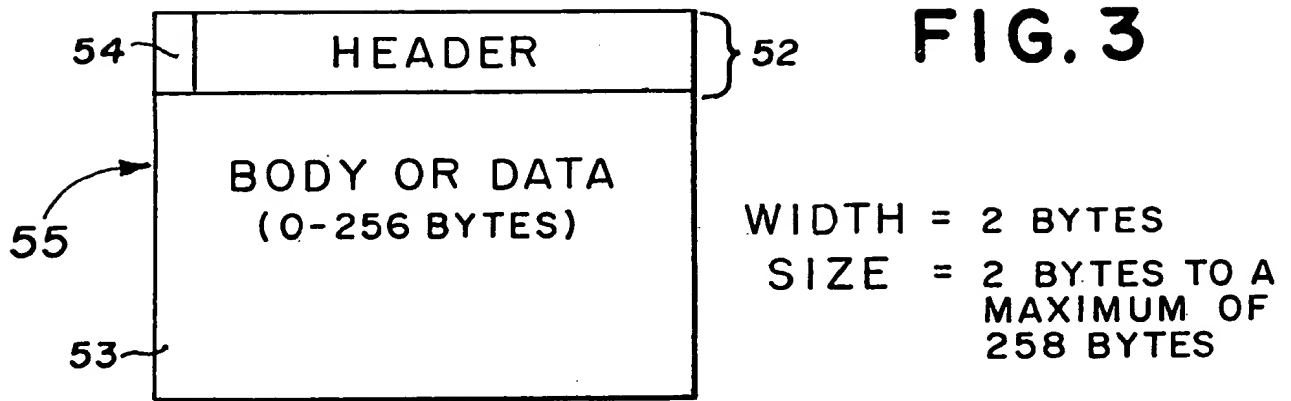
+



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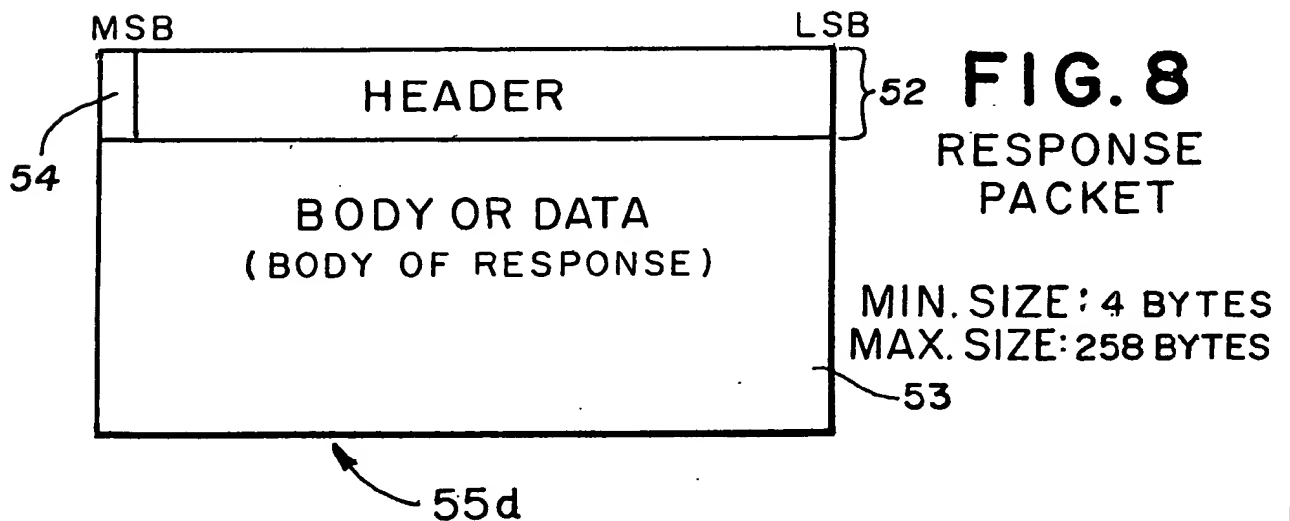
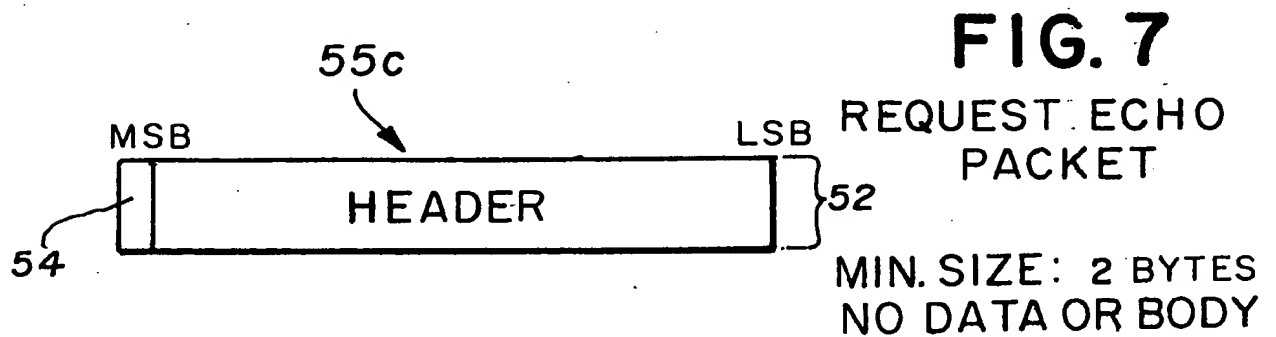
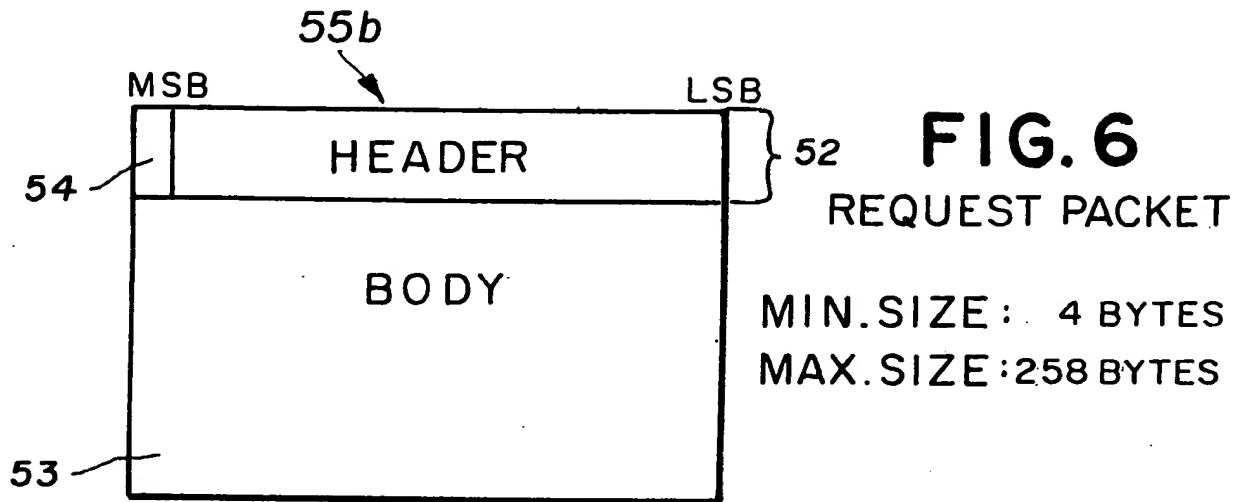


+



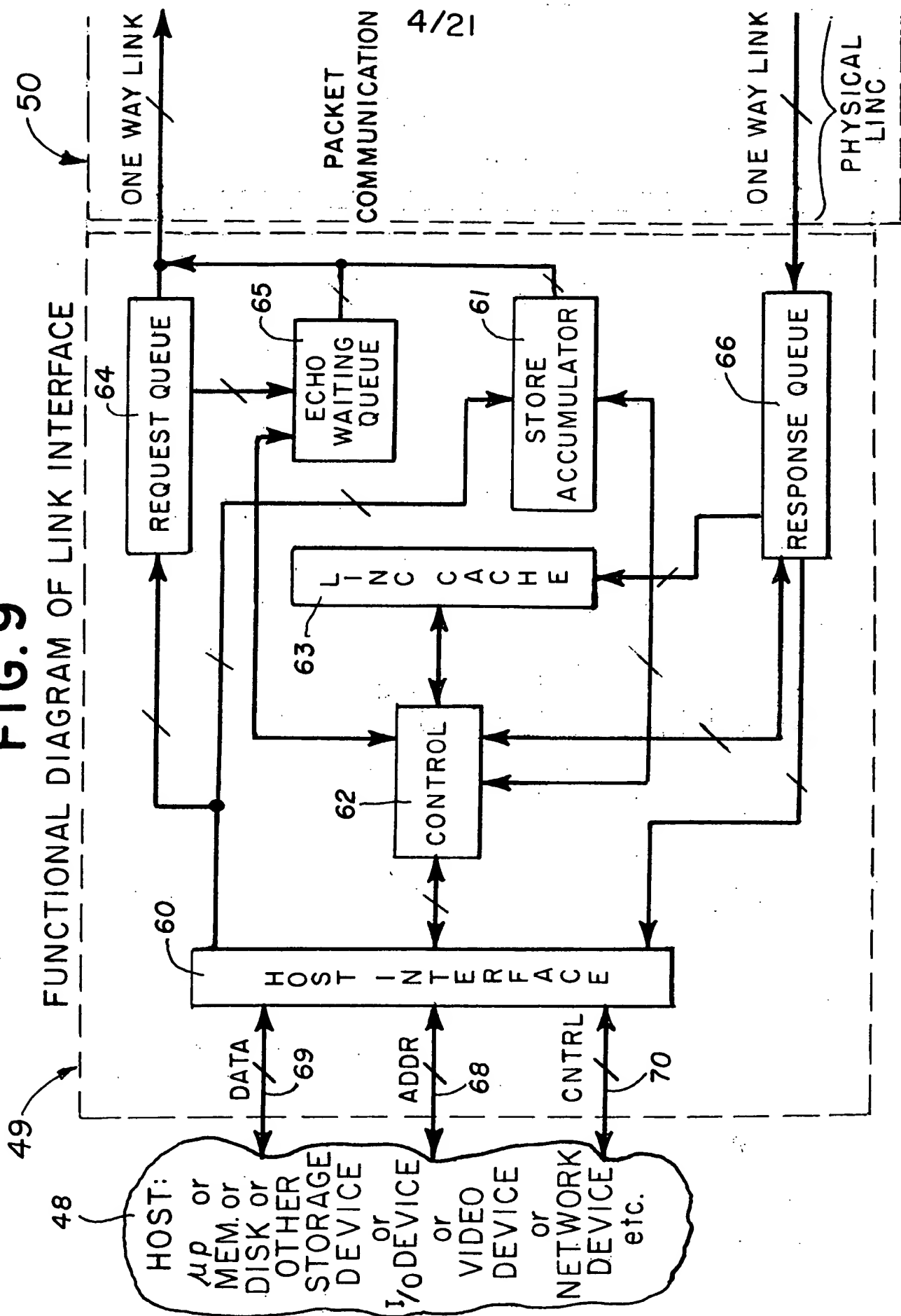
+

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+

FIG. 9

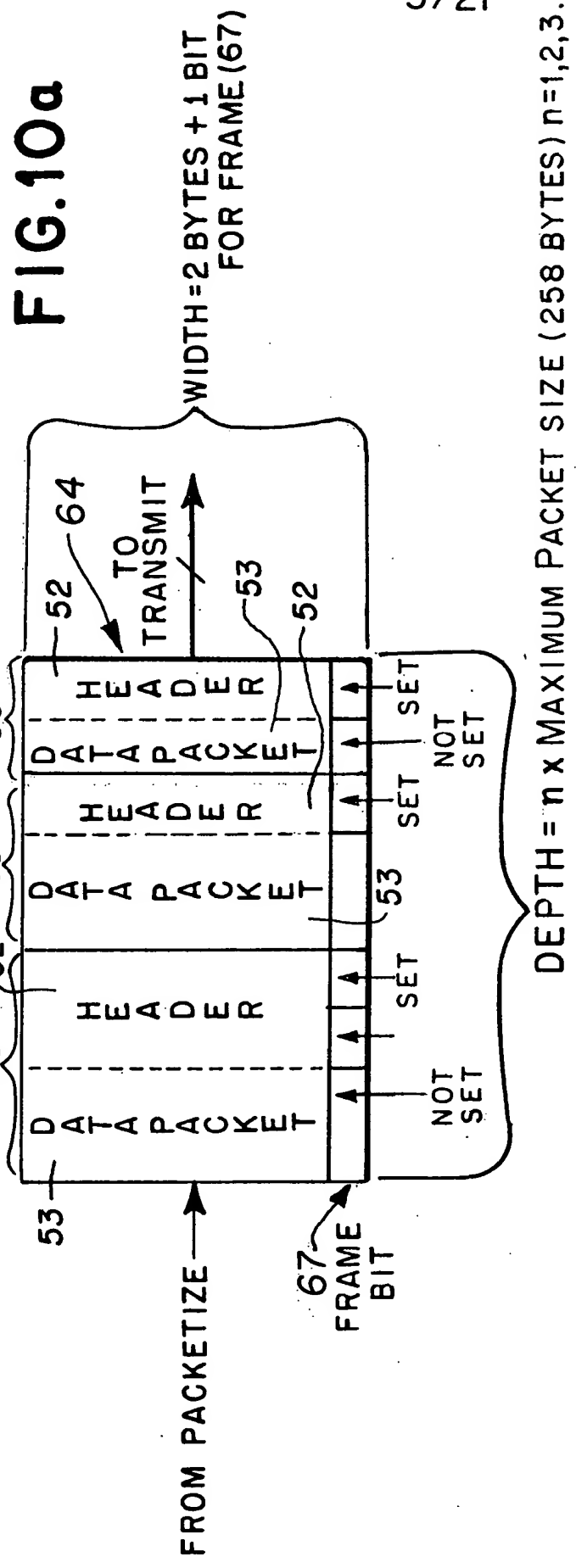


+

POSSIBLE REQUEST QUEUE STRUCTURES

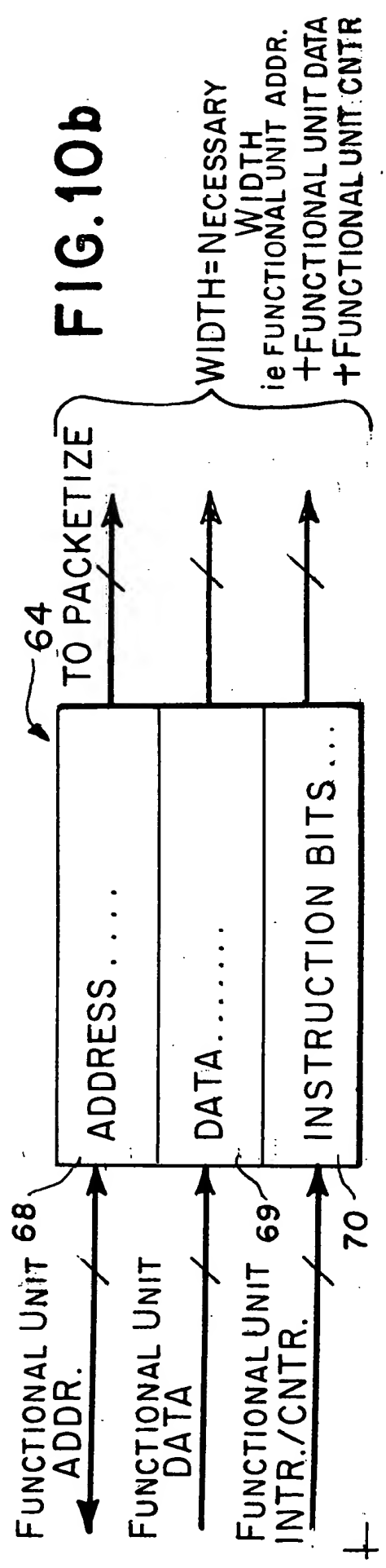
3rd. PACKET 2nd. PACKET 1st. PACKET

FIG. 10a



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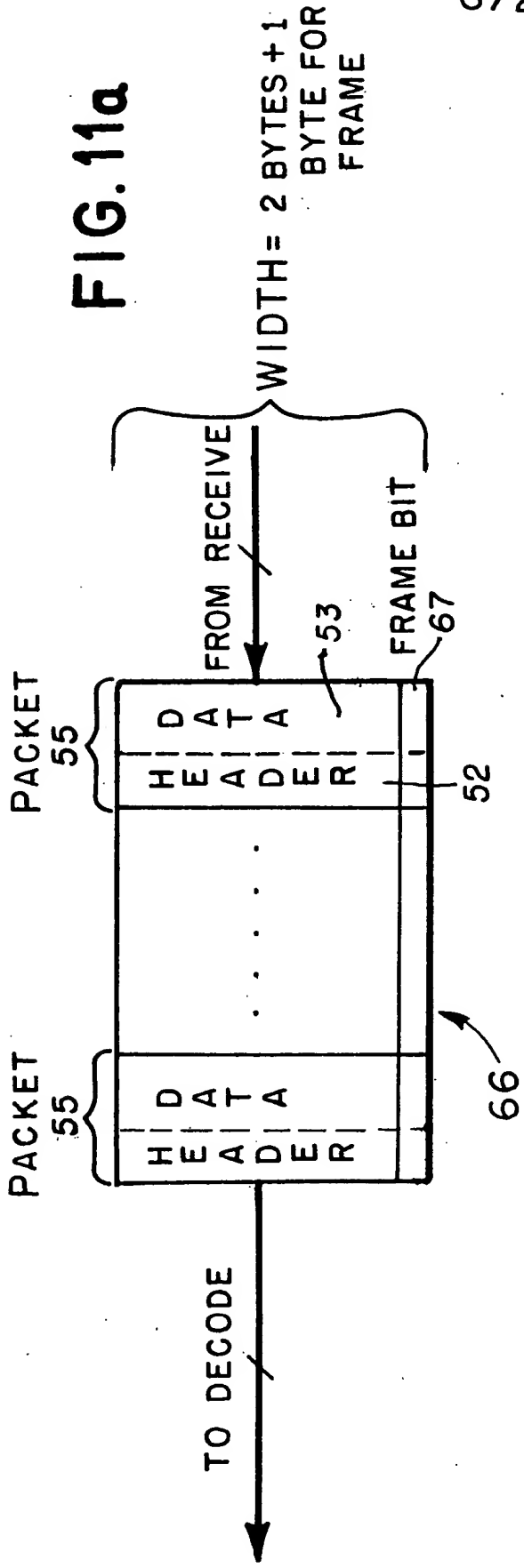
FIG. 10b



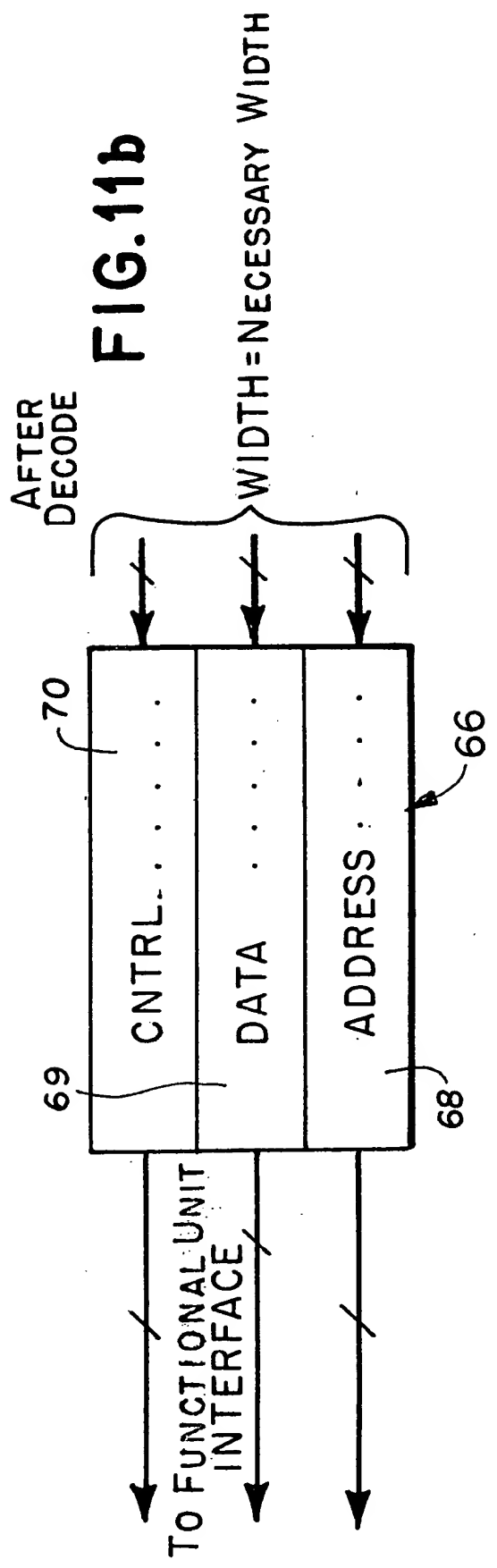
+

+

POSSIBLE RESPONSE QUEUE STRUCTURES

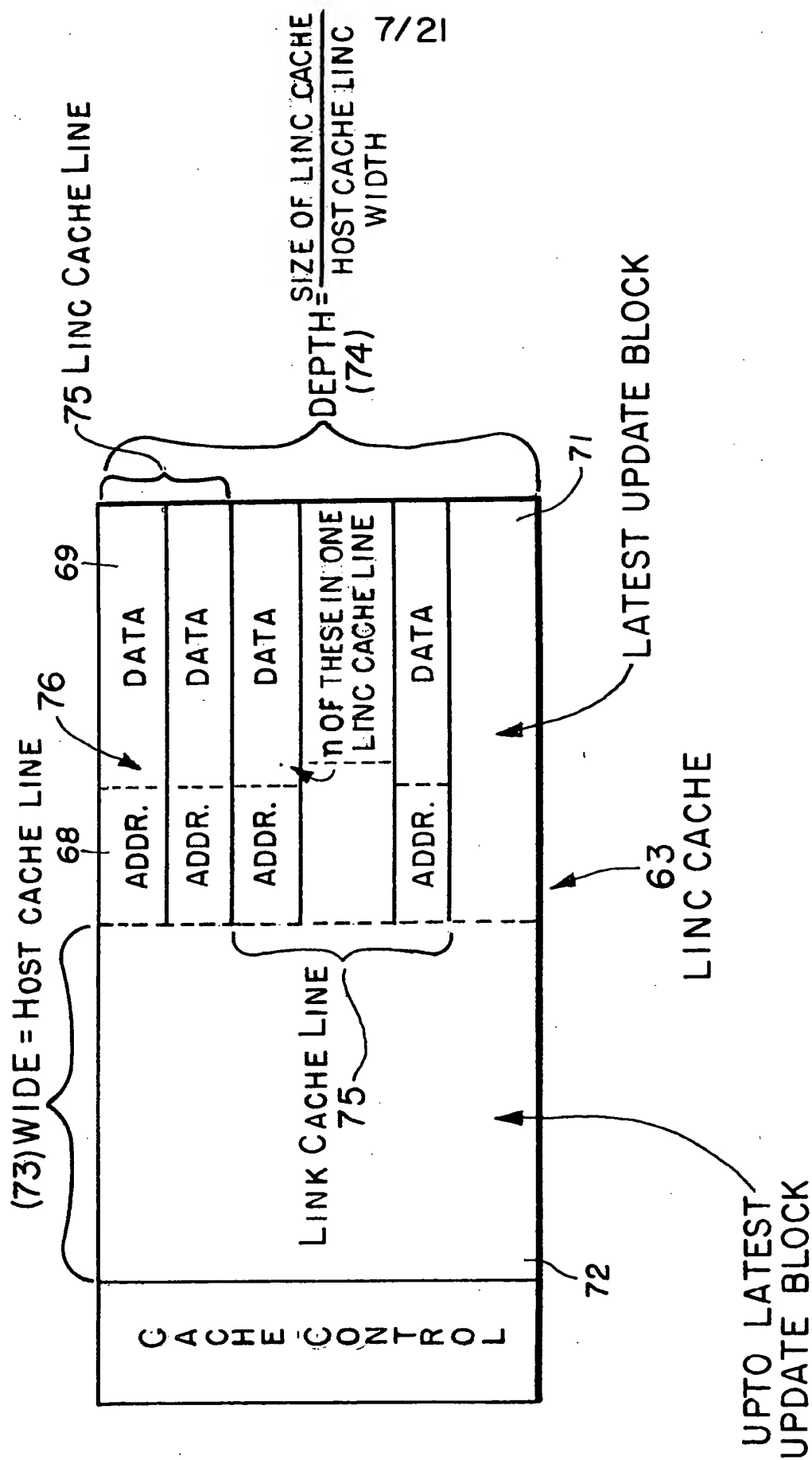


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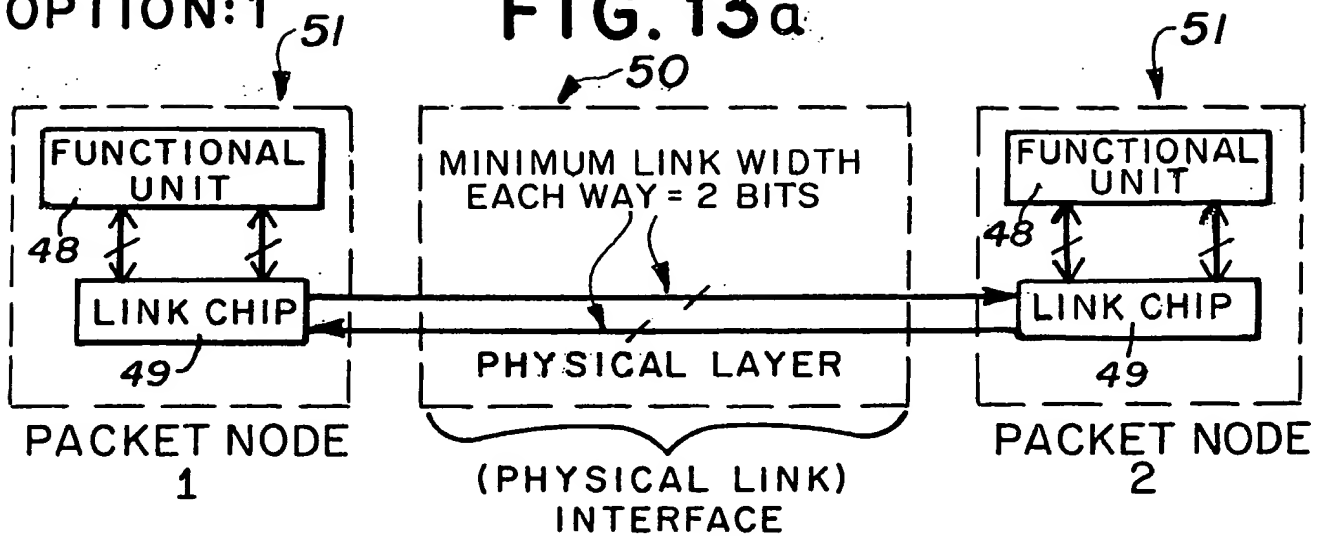
+

FIG. 12



OPTION:1

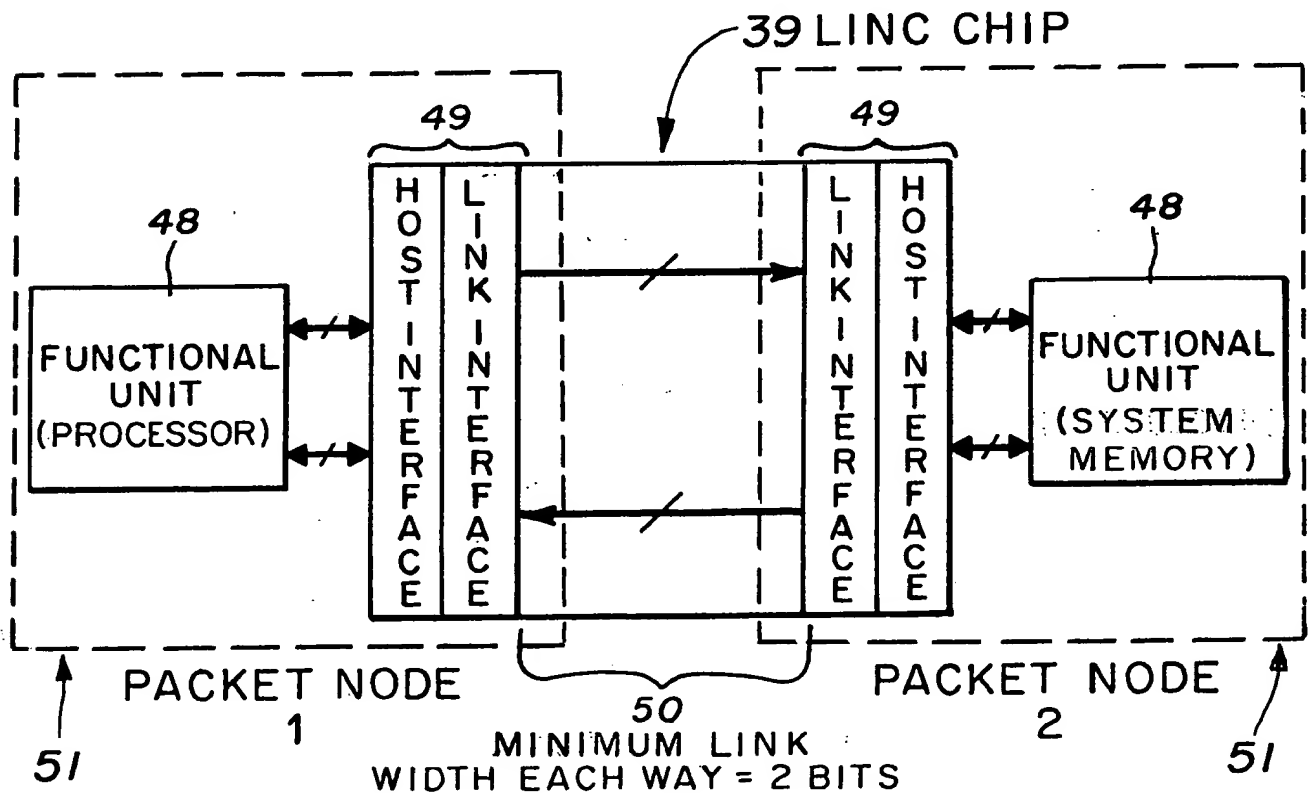
FIG. 13a



A SAMPLE TWO NODE LINK WHERE NODE 1 FUNCTIONAL UNIT IS THE PROCESSOR AND NODE 2 FUNCTIONAL UNIT IS THE MEMORY.

OPTION:2

FIG. 13b



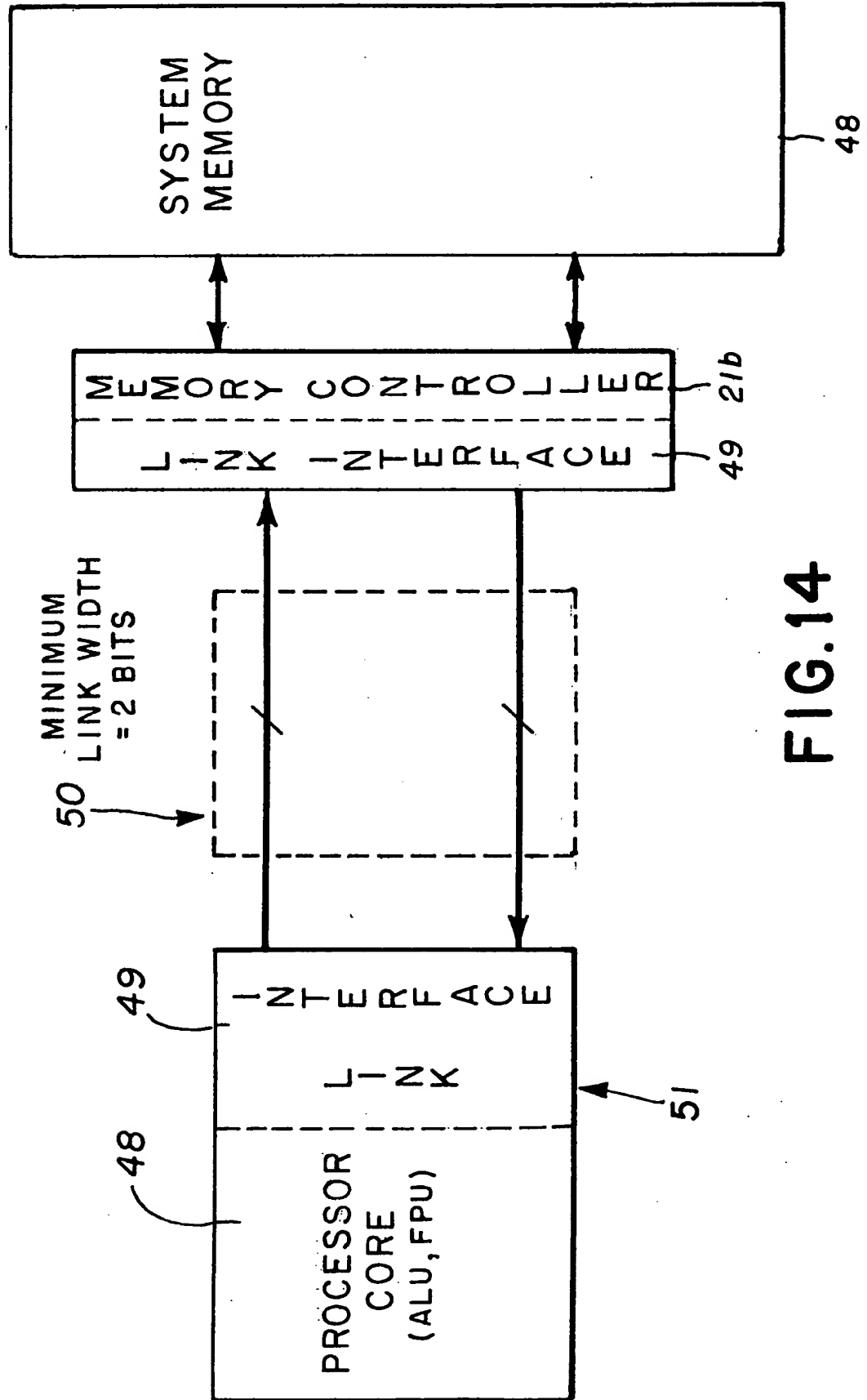


FIG.14

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FIG. 15

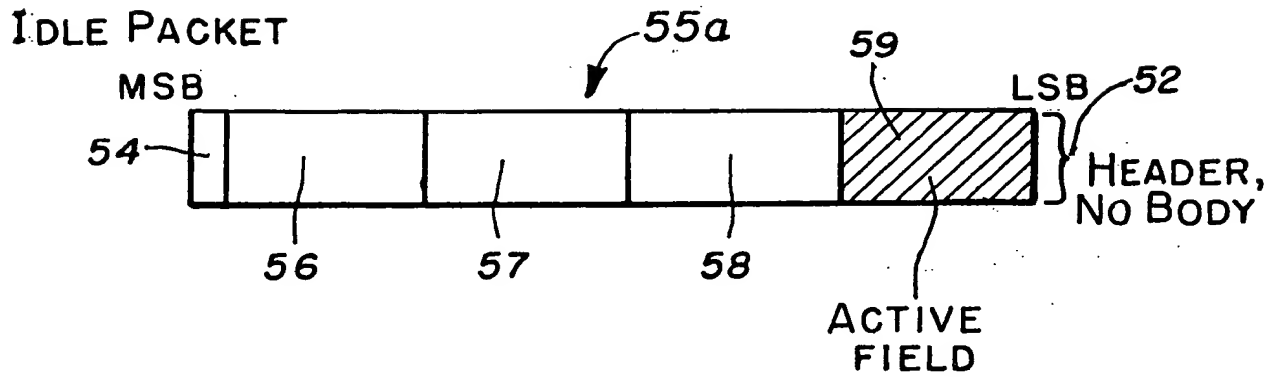


FIG. 16

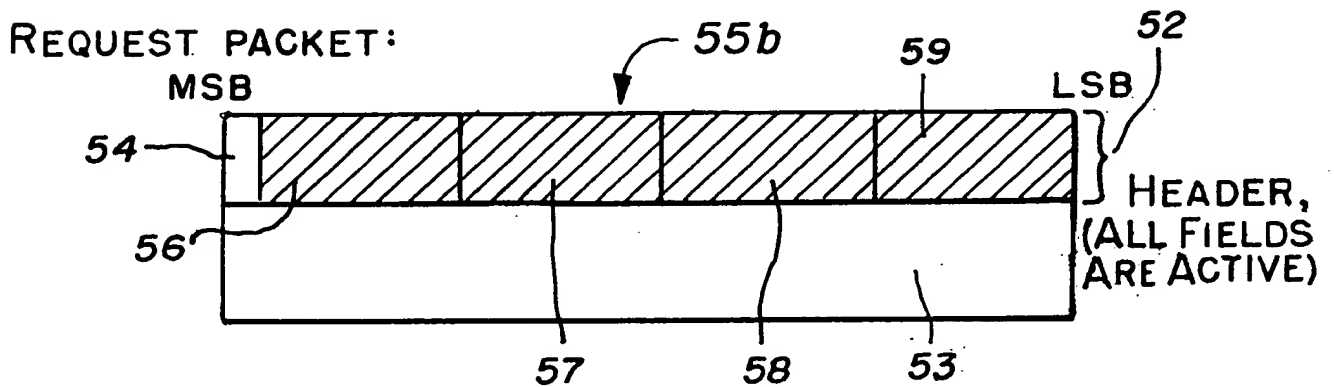
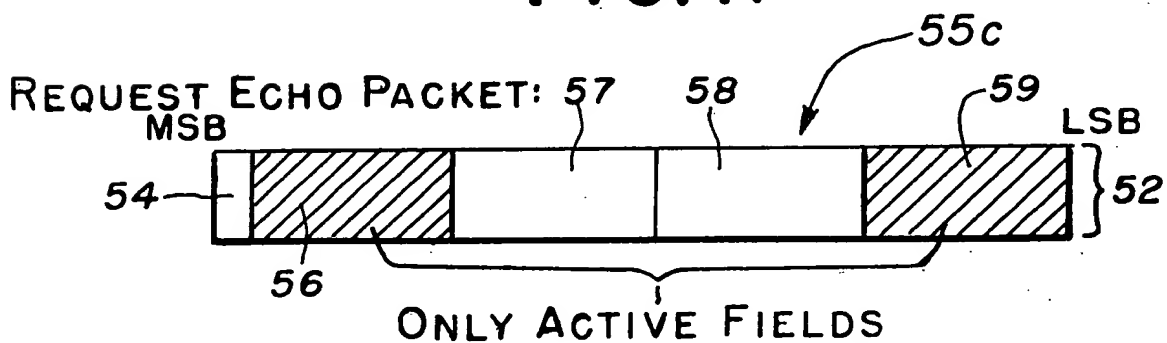


FIG. 17



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FIG. 18

RESPONSE PACKET

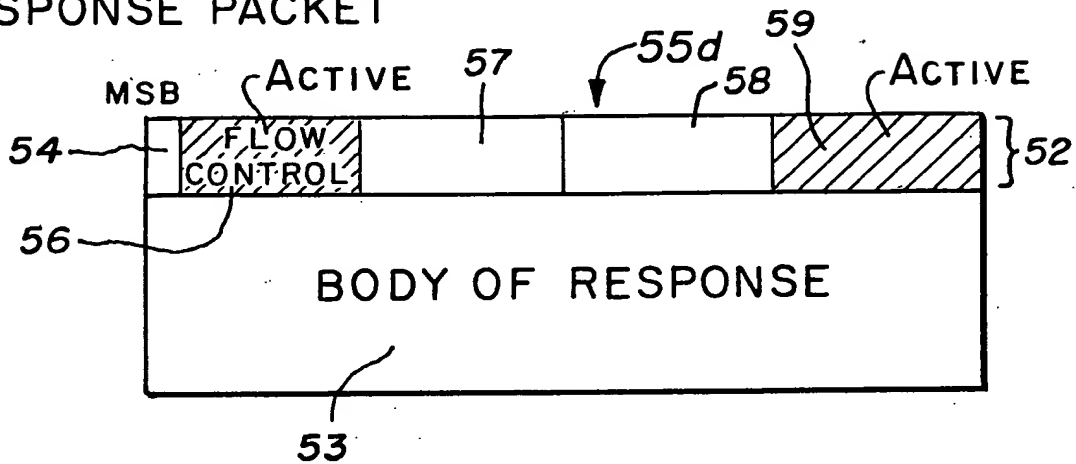
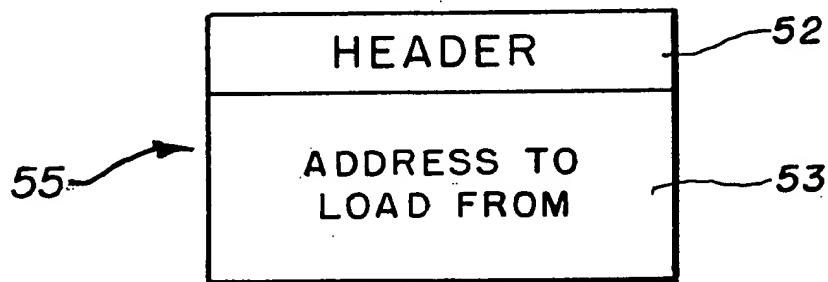
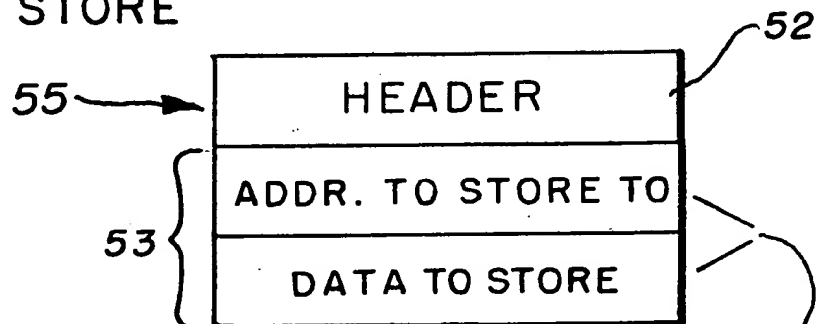


FIG. 19

REQUEST PACKET
FOR A LOAD



REQUEST PACKET
FOR A STORE



K OF EACH WHERE K IS
THE NUMBER OF STORES
IN THE STORE ACCUMU-
LATOR.

FIG. 20

HOST CHIP TRANSMIT HALF

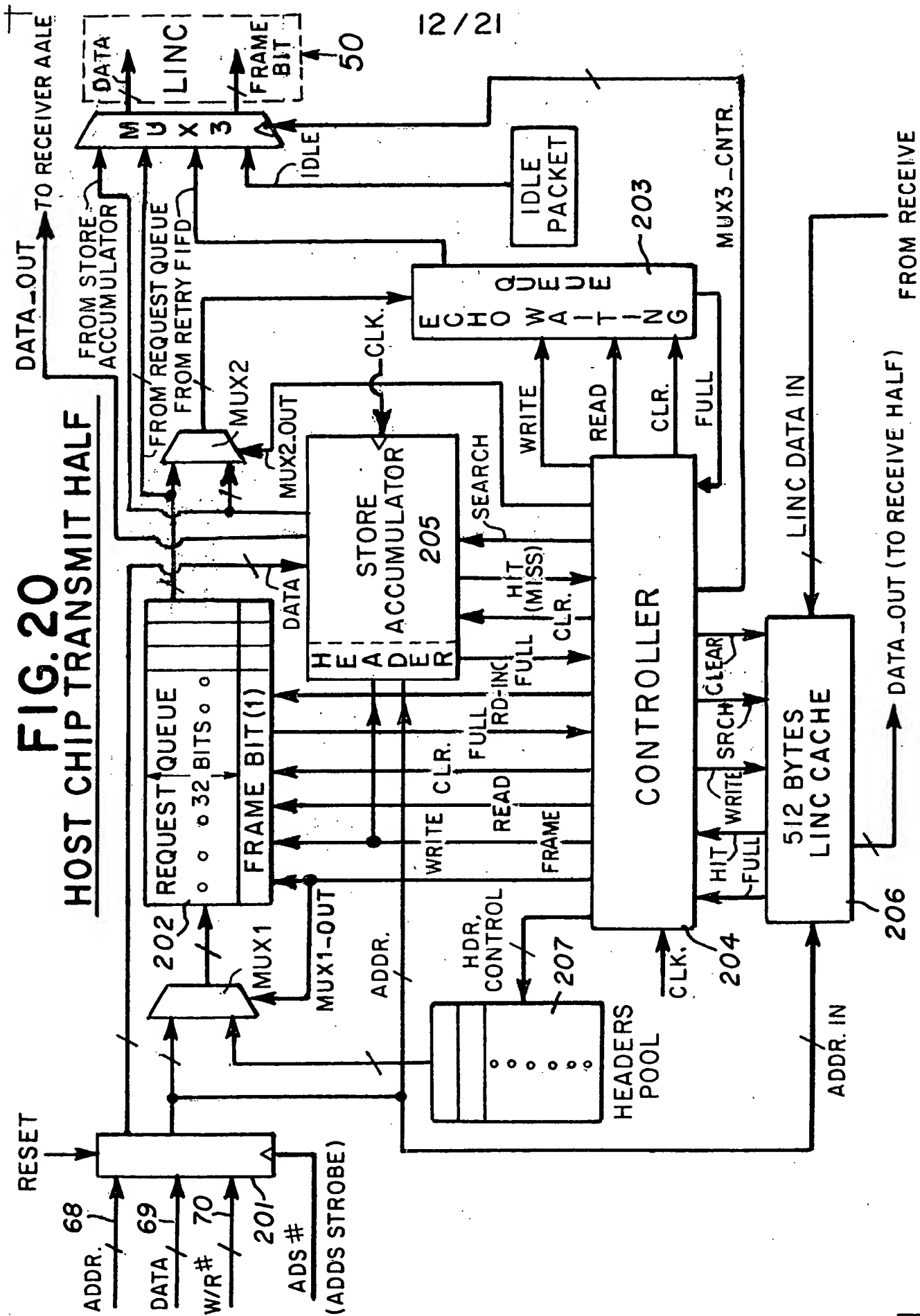


FIG. 21

RECEIVE HALF HOST CHIP

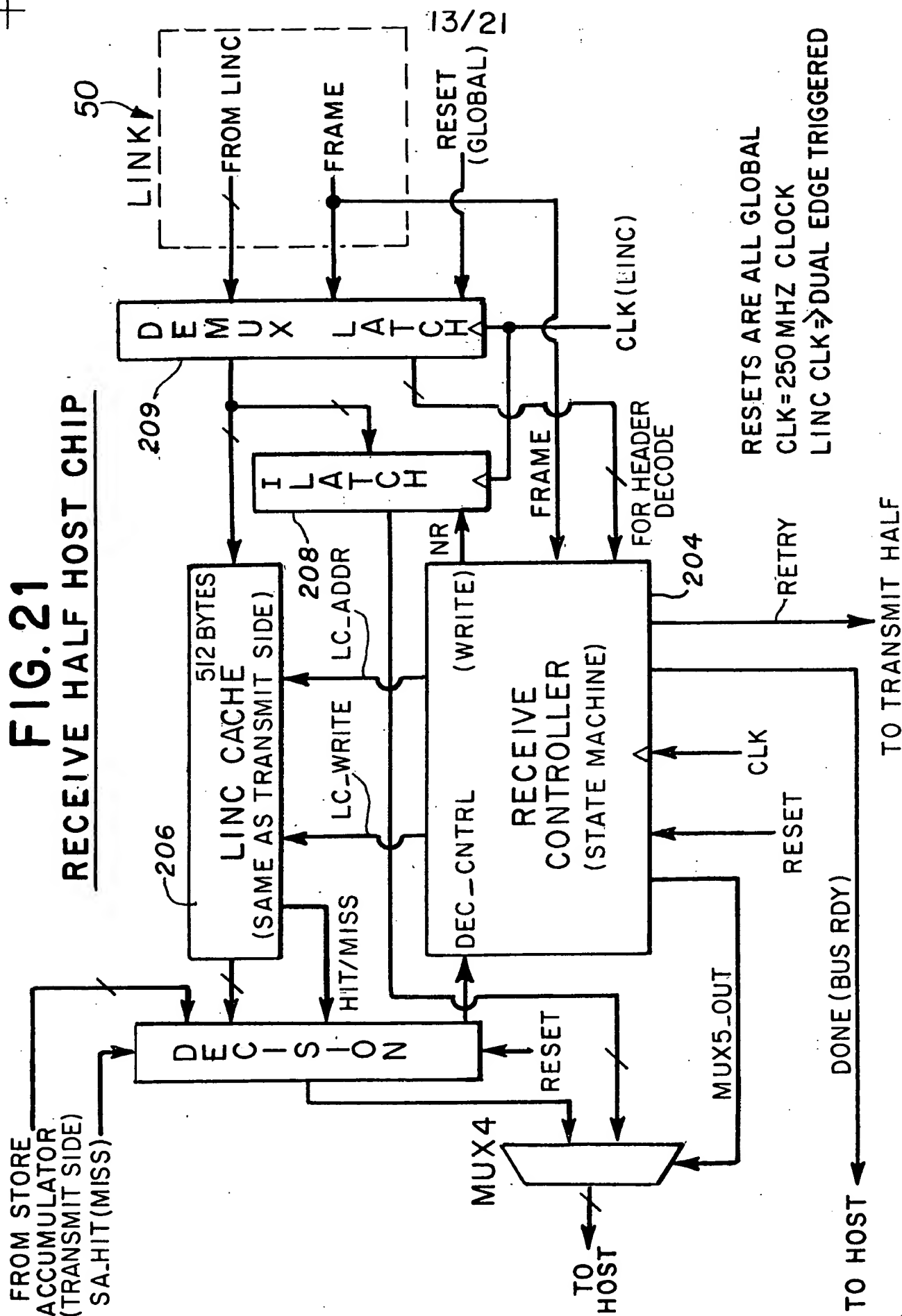


FIG. 22

MEMORY CHIP RECEIVE HALF

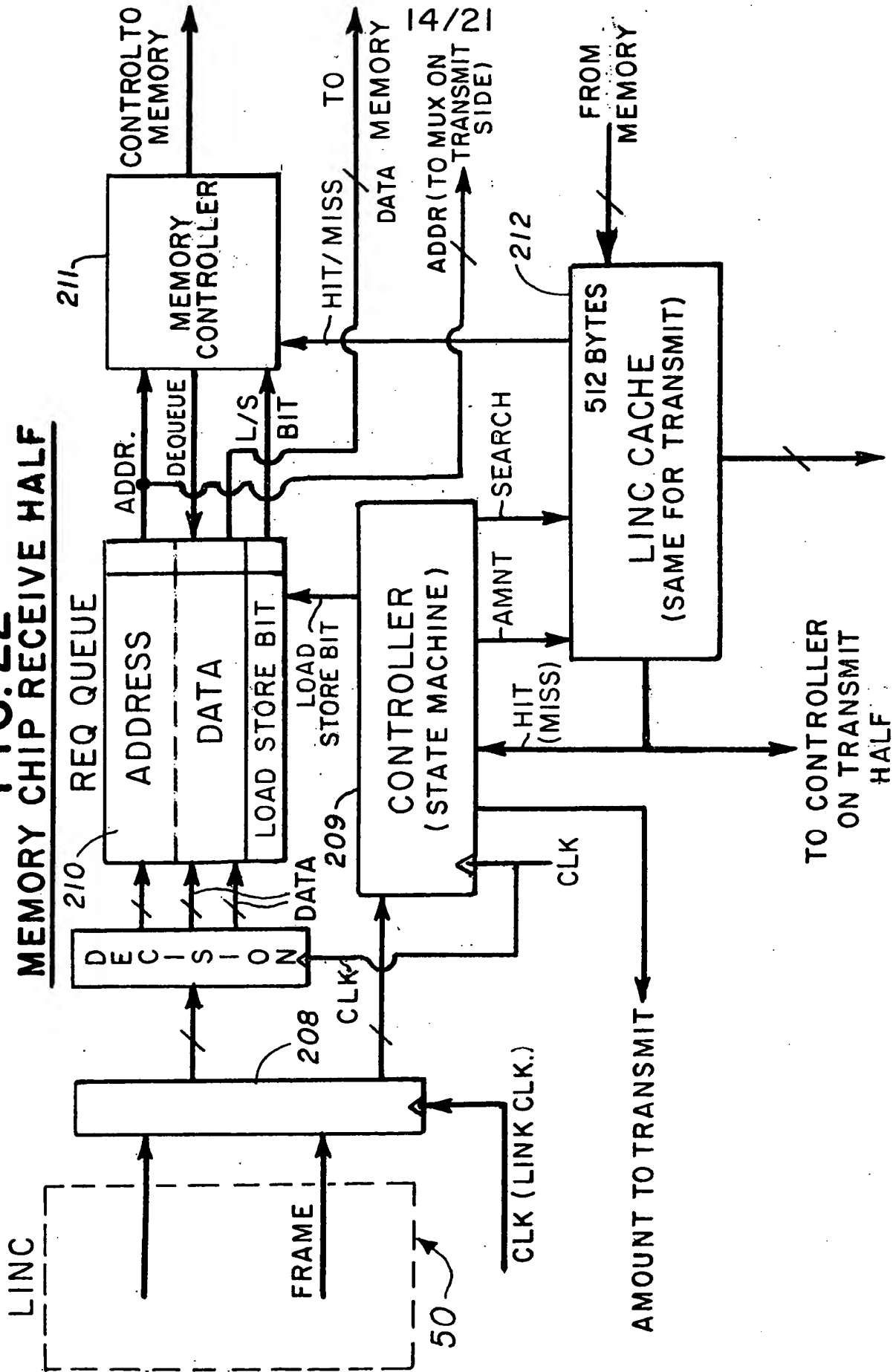
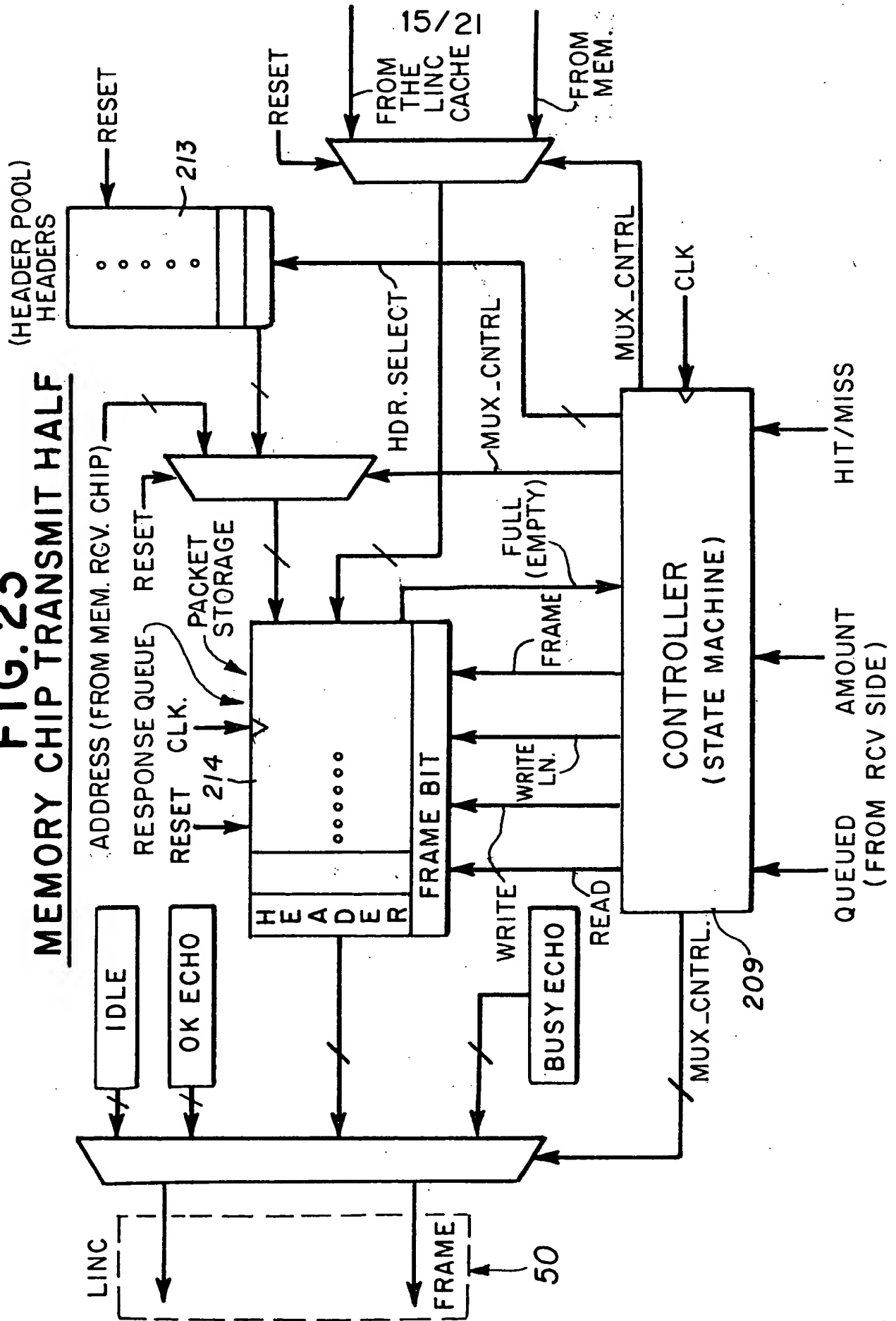


FIG. 23

MEMORY CHIP TRANSMIT HALF



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FIG. 24

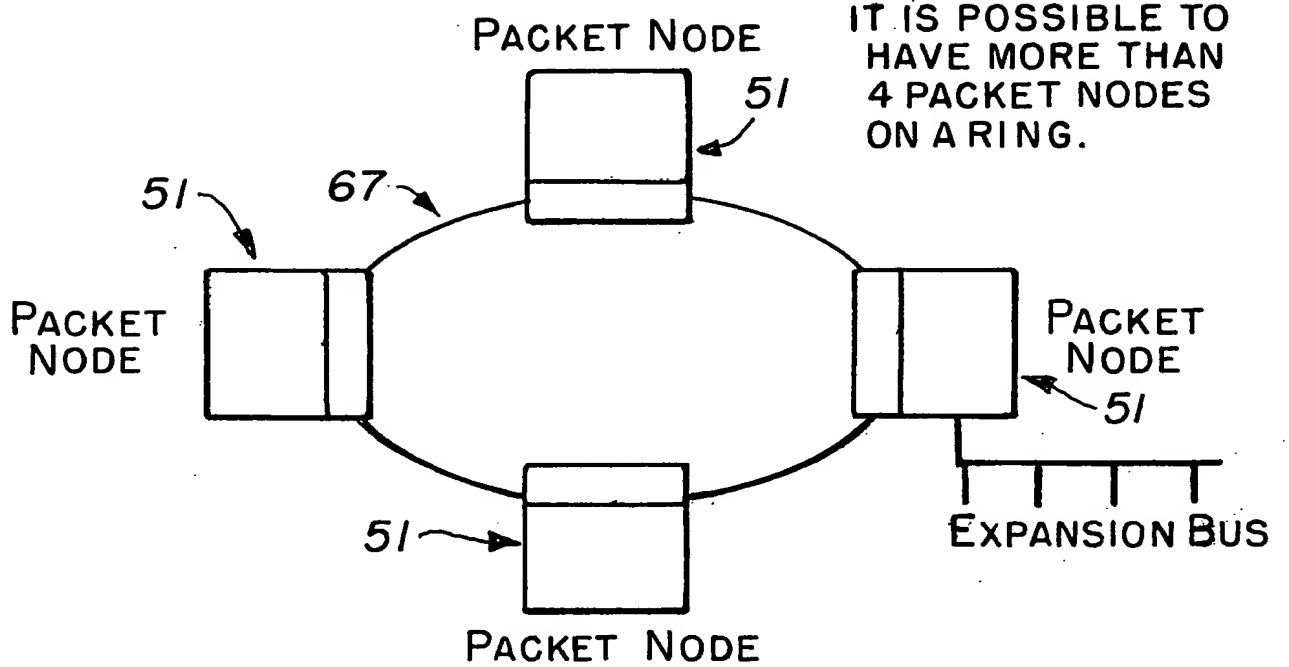
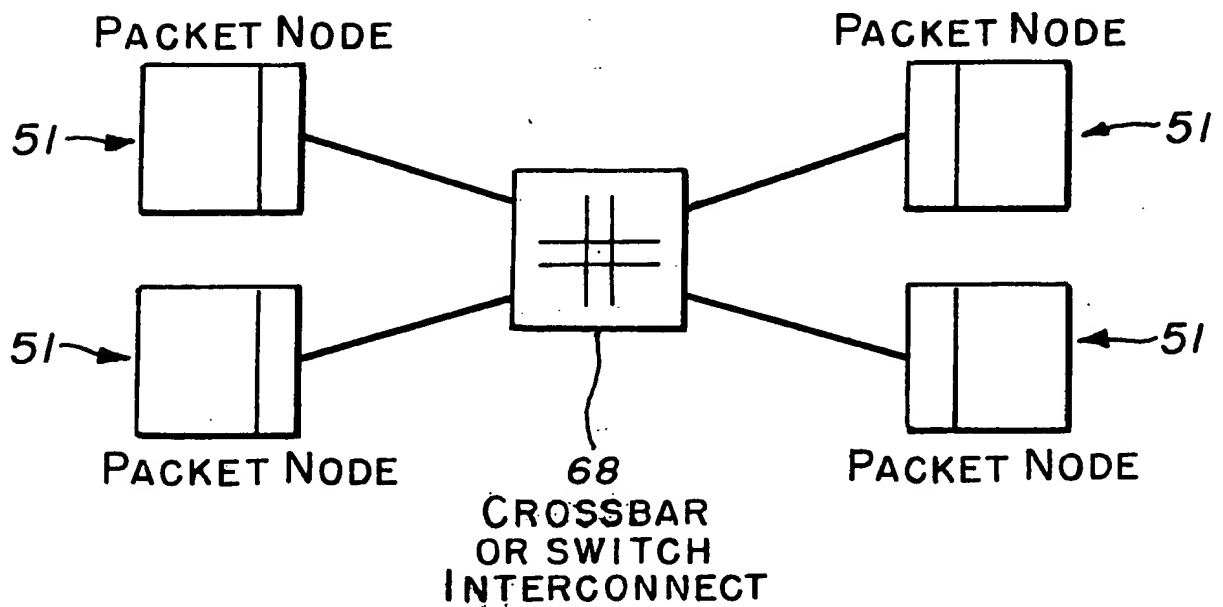
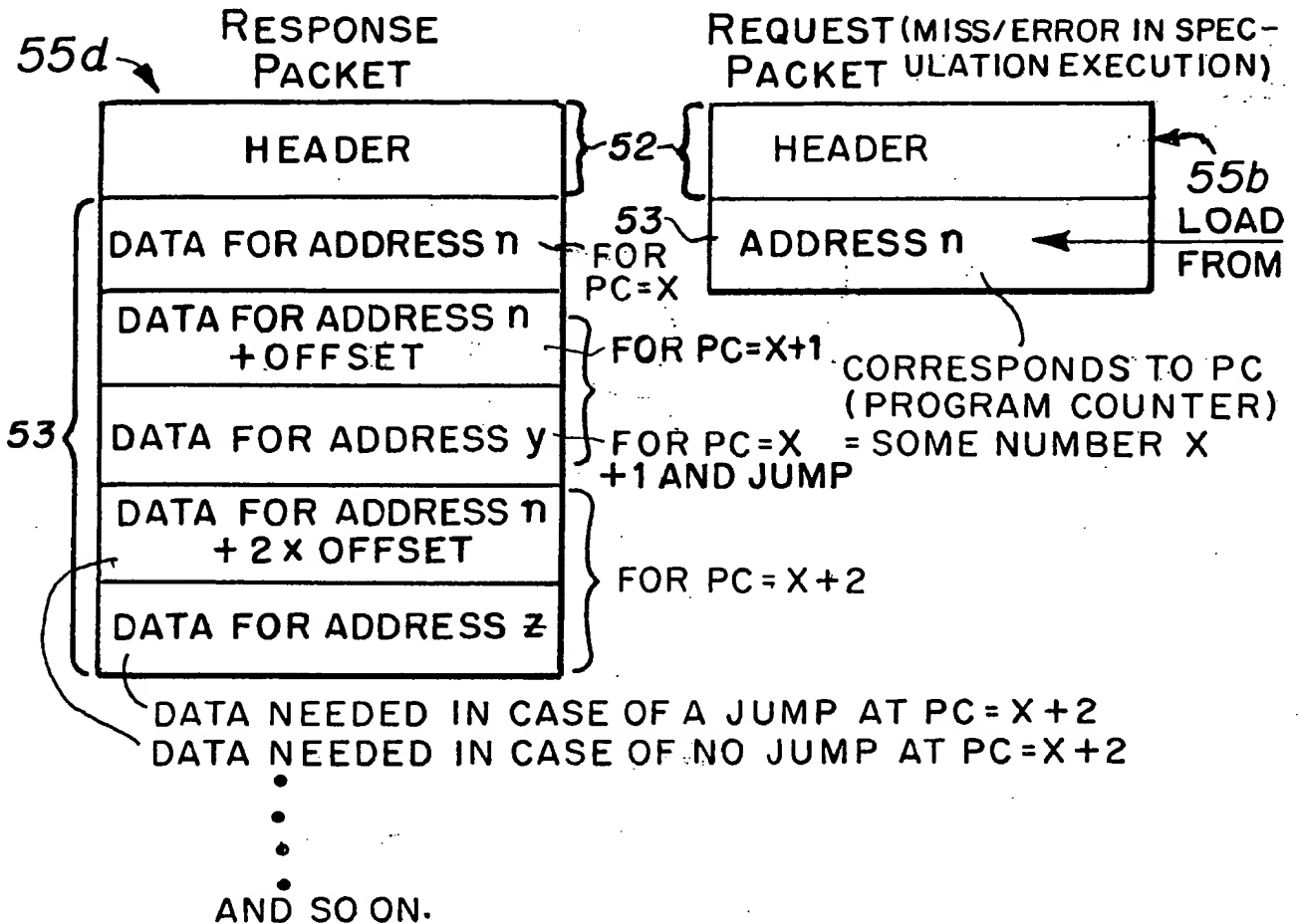


FIG. 25

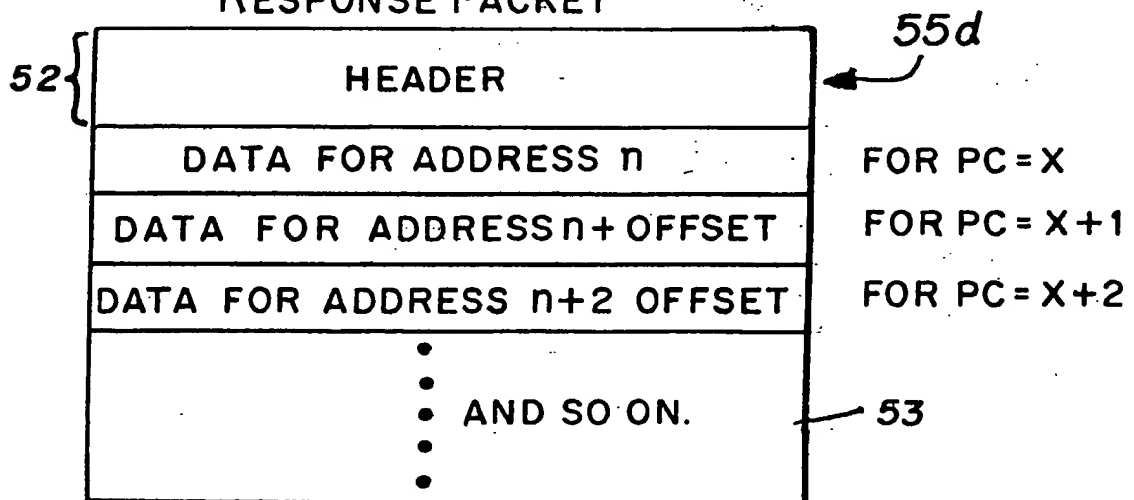


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FIG. 26

POSSIBLE RESPONSE PACKETS FOR A REQUEST
 WHEN ACCESS TO TLB AND OR BTB IN THE
 PROCESSOR IS AVAILABLE



FOR PROGRAMS WITH VERY HIGH LOCALITY
 (GRAPHICS, MULTIMEDIA ETC.)
 RESPONSE PACKET



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FIG. 27

PROCESSOR NODE RECEIVE PROTOCOL

FOR PRESENT DETAILED IMPLEMENTATION, THE MEMORY NODE IS EXPECTED TO SEND ONLY THE FOLLOWING PACKETS.

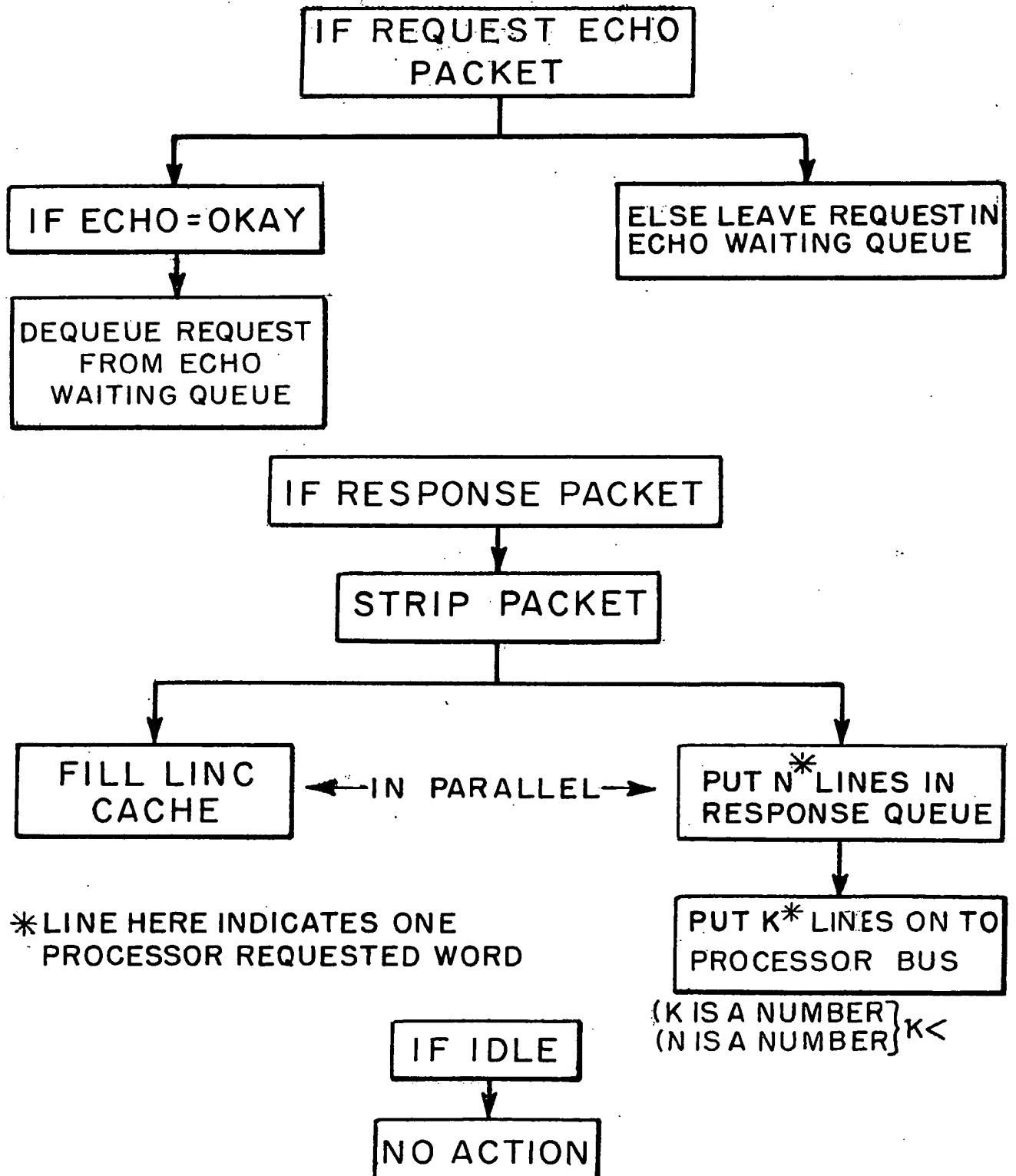
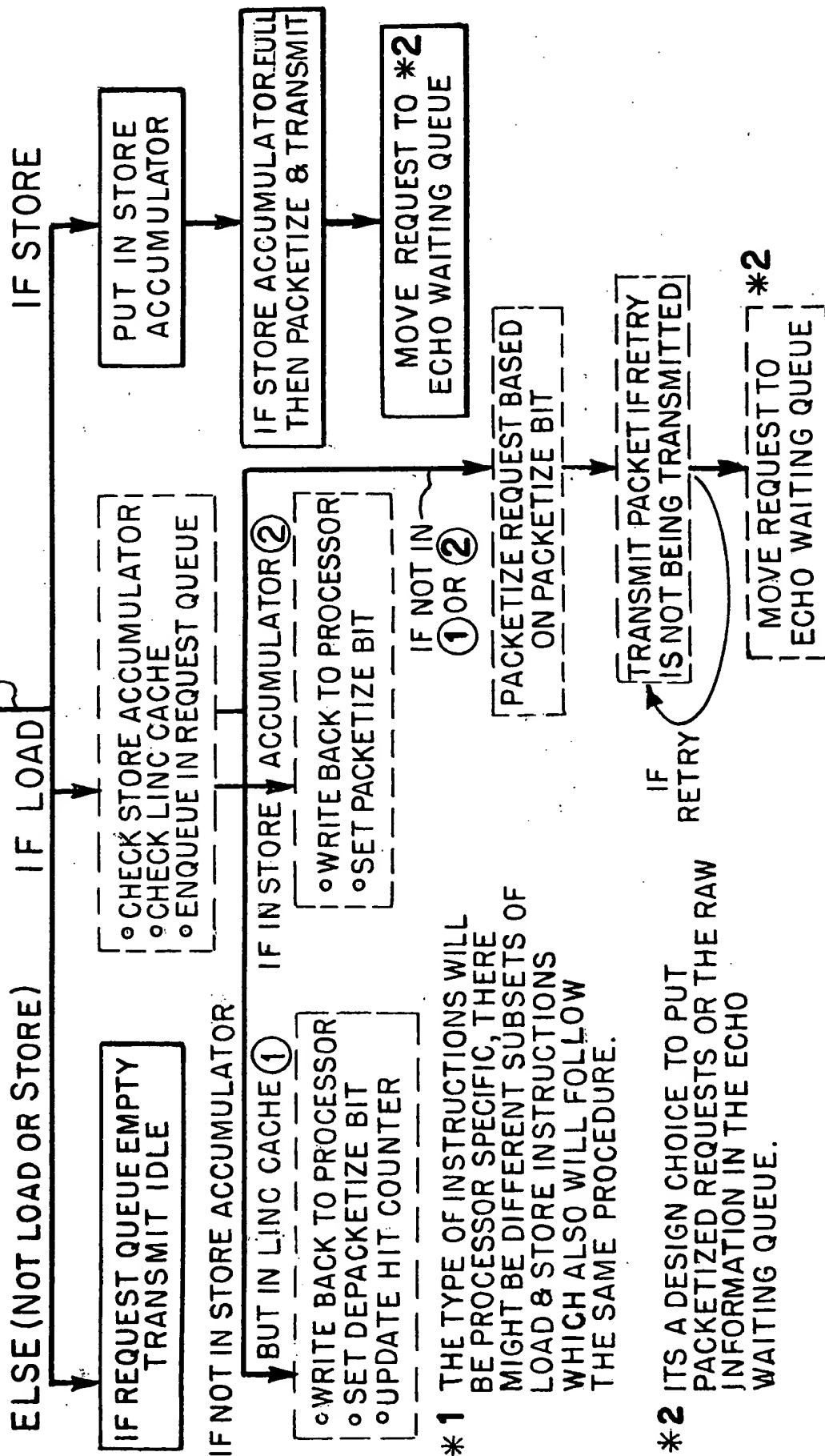


FIG. 28

PROCESSOR NODE TRANSMIT PROTOCOL

ALL ACTIONS WITHIN [] HAPPEN IN PARALLEL

CHECK LOAD OR STORE *1



*1 THE TYPE OF INSTRUCTIONS WILL BE PROCESSOR SPECIFIC, THERE MIGHT BE DIFFERENT SUBSETS OF LOAD & STORE INSTRUCTIONS WHICH ALSO WILL FOLLOW THE SAME PROCEDURE.

*2 ITS A DESIGN CHOICE TO PUT PACKETIZED REQUESTS OR THE RAW INFORMATION IN THE ECHO WAITING QUEUE.

FIG. 29

MEMORY NODE RECEIVE PROTOCOL

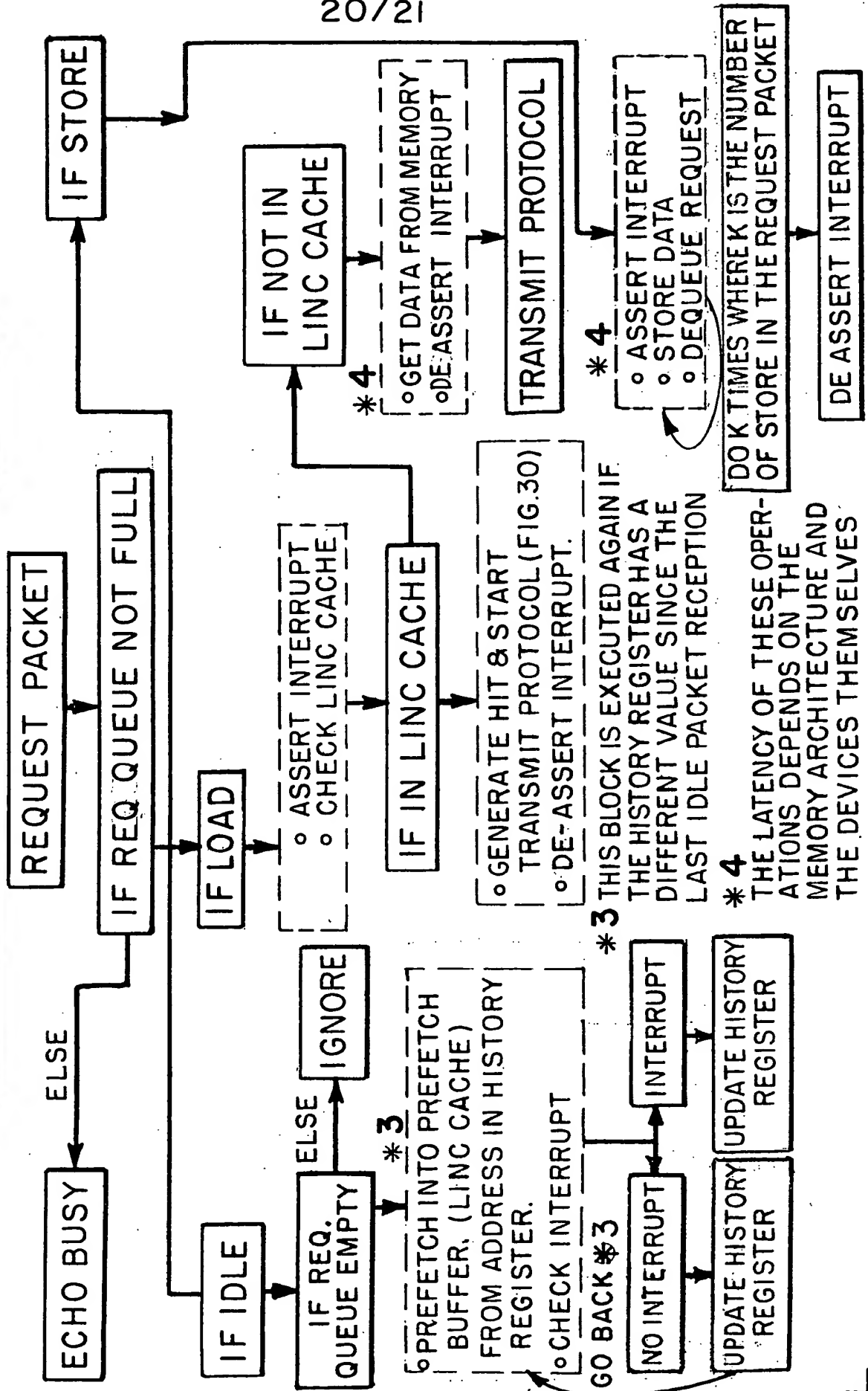


FIG. 30
MEMORY NODE TRANSMIT PROTOCOL

